IN THE CLAIMS

This Listing of Claims will replace all prior versions, and listings, of the claims:

Listing of Claims

1. (Currently Amended) A magnetic memory array comprising:

a plurality of bit cells, each bit cell including at least one magnetic layer having free magnetic poles with a corresponding demagnetization field; and

a magnetic flux absorbing layer having an isotropic response to magnetic fields disposed between at least two of the plurality of bit cells.

2. (Original) The magnetic memory array of claim 1, wherein the plurality of bit cells are oriented in rows and columns.

3. (Original) The magnetic memory array of claim 2, wherein the magnetic flux absorbing layer is disposed between at least one of the rows and the columns of the bit cells.

4. (Original) The magnetic memory array of claim 1, wherein the magnetic flux absorbing layer is disposed between all of the plurality of bit cells.

5. (Original) The magnetic memory array of claim 1, wherein the magnetic flux absorbing layer is substantially coplanar with the plurality of bit cells.

6. (Original) The magnetic memory array of claim 1, wherein the magnetic memory array is a magnetic random access memory array.

7. (Original) The magnetic memory array of claim 1, wherein the magnetic flux absorbing layer is contiguous with a non-magnetic layer.

8. (Original) The magnetic memory array of claim 1, wherein the magnetic flux absorbing layer is selected from the group consisting of iron, nickel, cobalt, alloys of iron, alloys of nickel, and alloys of cobalt.

9. (Original) The magnetic memory array of claim 1, wherein the magnetic flux absorbing layer is electrically insulating.

10. (Original) The magnetic memory array of claim 9, wherein the electrically insulating magnetic flux absorbing layer is a ferrite.

11. (Original) The magnetic memory array of claim 1, wherein the magnetic flux absorbing layer has a magnetic permeability of greater than 100.

12. (Original) The magnetic memory array of claim 1, wherein the magnetic flux absorbing layer has a coercivity of less than 10 Oersteds.

13. (Original) The magnetic memory array of claim 1, wherein the magnetic flux absorbing layer is an amorphous metal.

14. (Original) The magnetic memory array of claim 1, wherein the bit cells are spin tunneling bit cells.

15. (Currently Amended) A method of reducing demagnetization fields in a memory device having a plurality of magnetic bit cells, the method comprising:

depositing a magnetic flux absorbing layer having an isotropic response to magnetic fields at least between two bit cells of the plurality of bit cells.

16. (Original) The method of reducing demagnetization fields in a memory device of claim 15, wherein depositing the magnetic flux absorbing layer comprises depositing an electrically

insulating magnetic flux absorbing layer.

17. (Original) The method of reducing demagnetization fields in a memory device of claim 15, wherein depositing the magnetic flux absorbing layer comprises depositing material selected from the group consisting of iron, nickel, cobalt, alloys of iron, alloys of nickel, and alloys of cobalt.

18. (Canceled)

19. (Original) The method of reducing demagnetization fields in a memory device of claim 15, further comprising depositing a non-magnetic layer at least between two of the bit cells.

20. (Currently Amended) A memory chip separated from a memory wafer and configured for use in an electronic device, the memory chip comprising:

at least one memory array having a plurality of bit cells, each bit cell including at least one magnetic layer having free magnetic poles and a corresponding demagnetization field; and

magnetic flux absorbing means having an isotropic response to magnetic fields between adjacent bit cells.

21. (Original) The memory chip of claim 20, wherein the magnetic flux absorbing means between adjacent bit cells is a coating deposited between adjacent bit cells, the coating comprising at least one non-magnetic layer contiguous with at least one magnetic flux absorbing layer.

22. (Original) The memory chip of claim 20, wherein the magnetic flux absorbing means between adjacent bit cells is an electrically insulating soft magnetic material.

23. (Currently Amended) An electronic system comprising:

an electronic device; and

a memory chip electrically connected to the electronic device, the memory chip including a memory array;

wherein the memory array includes a plurality of bit cells and

a magnetic flux absorbing layer having an isotropic response to magnetic fields disposed between at least two of the plurality of bit cells.